WHAT IS CLAIMED IS:

1. A microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the microcomputer comprising:

an input and output circuit having a plurality of operation modes;

a control signal generator for generating a write signal in an operation mode setting routine of the control program;

a control circuit for setting an operation mode of the input and output circuit in response to the write signal; and

a protection circuit for protecting the input and output circuit from being reset in operation mode until the protection circuit is reset by the reset signal from the outside once the control circuit has set the operation mode,

wherein the input and output circuit receives a signal from and sends a signal to the outside in accordance with the operation mode set by the control circuit.

2. An operation mode control circuit in a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator;

a write protection circuit for generating a buffer signal in response to only a first output signal the control signal generator outputs first subsequent to the reset of the microcomputer; and

a control circuit for latching a second output signal from the control signal generator in response to the buffer signal from the write protection circuit,

wherein the control circuit sets an operation mode of an input and output circuit, which receives a signal from and

sends a signal to the outside, in accordance with the latched second output signal.

3. An operation mode control circuit as claimed in claim 2, wherein the first output signal comprises a pulse signal.

4. An operation mode control circuit as claimed in claim 2, wherein the write protection circuit comprises:

buffer units for outputting a buffer signal that is a buffered version of the first output signal or a fixed logical value signal in response to the first output signal output from the control signal generator; and

latch units for performing a latch process in response to the first output signal from the control signal generator and for outputting a status signal indicating a latch status thereof,

wherein the buffer units has an input terminal for receiving the status signal from the latch units, and outputs the fixed logical value signal if the status signal indicates the latch status, or outputs the buffer signal if the status signal does not indicate the latch status.

5. An operation mode control circuit as claimed in claim 2, wherein the write protection circuit comprises:

an AND gate for receiving the first output signal from the control signal generator at one of input terminals thereof;

a flip-flop, with the latch terminal thereof connected to an output terminal of the AND gate, for outputting a signal having a logical signal "1" when a pulse signal is received at the latch terminal thereof; and

a buffer for outputting a logically inverted version of a signal from the flip-flop to the other of the input terminals of the AND gate,

wherein the AND gate AND gates the first output signal from the control signal generator and the logically inverted version of the signal from the flip-flop.

6. A microcomputer, comprising:

an operation mode control circuit, wherein the operation mode control circuit includes a control signal generator, a write protection circuit for generating a buffer signal in response to only a first output signal the control signal generator outputs first subsequent to the reset of the microcomputer, and a control circuit for latching a second output signal from the control signal generator in response to the buffer signal from the write protection circuit;

an input and output circuit for receiving a signal from and sending a signal to the outside; and

a data register for latching a data signal from the operation mode control circuit in response to a data register write signal from the operation mode control circuit,

wherein the data register outputs, to the input and output circuit, a signal responsive to the data signal.

7. An operation mode control circuit in a microcomputer for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator;

a write protection circuit for generating a buffer signal that is a buffered version of a first output signal from the control signal generator only if a first decode signal and a second decode signal have been successively received from the control signal generator; and

a control circuit for latching a second signal from the control signal generator in response to the buffer signal from the write protection circuit,

wherein the control circuit sets, in response to the second output signal latched, the operation mode of an input and output control circuit that receives a signal from and sends a signal to the outside.

8. An operation mode control circuit as claimed in claim 7, wherein the first output signal comprises a pulse signal.

9. An operation mode control circuit in a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator;

a write protection circuit for generating a buffer signal that is a buffered version of a first output signal from the control signal generator only if a plurality of decode signals have been successively received from the control signal generator; and

a control circuit for latching a second signal from the control signal generator in response to the buffer signal from the write protection circuit,

wherein the control circuit sets, in response to the second output signal latched, the operation mode of an input and output control circuit that receives a signal from and sends a signal to the outside.

10. An operation mode control circuit as claimed in claim 7, wherein the write protection circuit comprises:

a decoder for outputting a first selection status signal and a second selection status signal in response to the first decode signal and the second decode signal from the control signal generator, respectively;

a first AND gate for receiving the first selection status

signal at one of input terminals thereof;

a second AND gate for receiving the second selection status signal at one of input terminals thereof;

a third AND gate;

a first flip-flop for latching an output signal from the first AND gate in response to the first output signal from the control signal generator and for outputting first data to the other of the input terminals of the second AND gate;

a second flip-flop for latching an output from the second AND gate in response to the first output signal from the control signal generator and for outputting second data to one of input terminals of the third AND gate; and

a buffer for outputting, to the other of the input terminals of the first AND gate, a third output signal that is a logically inverted version of the second data,

wherein the first AND gate AND gates the first election status signal and the third output signal,

wherein the second AND gate AND gates the second selection status signal and the first data,

wherein the third AND gate AND gates the second data and the first output signal, and

wherein the control circuit includes a third flip-flop that latches the second output signal from the control signal generator in response to an output signal from the third AND gate.

11. A microcomputer comprising:

an operation mode control circuit, wherein the operation mode control circuit includes a control signal generator, a write protection circuit for generating a buffer signal that is a buffered version of a first output signal from the control signal generator only if a first decode signal and a second decode signal have been received from the control signal

generator, and a control circuit for latching a second signal from the control signal generator in response to the buffer signal from the write protection circuit;

an input and output control circuit for controlling signal inputting from and signal outputting to the outside; and

a data register for latching a data signal from the operation mode control circuit in response to a data register write signal from the operation mode control circuit,

wherein the data register outputs a signal responsive to the data signal to the input and output control circuit.

12. An operation mode control circuit in a microcomputer for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator;

a write protection circuit for latching a second output signal from the control signal generator in response to a first output signal from the control signal generator, and for generating a write signal responsive to the logical value of the latched second output signal; and

a control circuit for latching a third output signal from the control signal generator in response to the write signal and for generating a control signal responsive to the logical value of the latched third output signal,

wherein the write signal responsive to the logical value of the second output signal from the control signal generator is a signal with the logical value fixed or a buffer signal that is the buffered version of the first output signal from the control signal generator, and

wherein the control signal is supplied to a selection circuit that selects one signal generator from among a plurality of signal generators, each containing at least a data register, for sending a signal to the outside.

13. An operation mode control circuit, in a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator;

a write protection circuit for latching a second output signal from the control signal generator in response to a first output signal from the control signal generator and generating a write signal responsive to the logical value of the latched second signal;

a first control circuit for latching a third output signal from the control signal generator in response to the write signal and for generating a first control signal responsive to the logical value of the latched third output signal;

a second control circuit for latching a fifth output signal from the control signal generator in response to a fourth output signal from the control signal generator, and for generating a second control signal responsive to the logical value of the latched fifth output signal;

an OR gate for OR gating the first control signal and the second control signal and outputting an OR gate output as an operation mode setting signal,

wherein the write signal responsive to the logical value of the second output signal from the control signal generator is a signal with the logical value thereof fixed or a buffer signal that is a buffered version of the first output signal from the control signal generator,

wherein the first control signal is supplied to a selection circuit that selects one signal generator from among a plurality of signal generators, each containing at least a data register, for sending a signal to the outside, and

wherein the operation mode setting signal is supplied to a

circuit, which controls signal inputting from and signal outputting to the outside, to set the operation mode of the circuit.

14. An operation mode control circuit as claimed in claim 12, wherein the write protection circuit comprises:

buffer units for outputting one of the buffer signal resulting from the first output signal and the signal having the fixed logical value in response to the first output signal from the control signal generator, and

latch units for latching the second output signal from the control signal generator in response to the buffer signal and outputting a logical signal responsive to the logical value of the second output signal,

wherein the buffer units receives the logical signal from the latch units, and outputs a signal with the logical value thereof fixed in response to one logical value of the logical signal while outputting the buffer signal in response to the other logical value of the logical signal.

15. An operation mode control circuit as claimed in claim 12, wherein the write protection circuit comprises:

an AND gate for receiving, at one of input terminals thereof, the first output signal from the control signal generator;

a buffer for outputting a buffer signal that is an logically inverted version of the second output signal from the control signal generator; and

a latch for receiving the buffer signal at a data terminal thereof, for latching the buffer signal in response to an output from the AND gate, and for generating a logical signal responsive to the logical value of the buffer signal,

wherein the AND gate AND gates the logical signal and the

first output signal.

16. A microcomputer comprising:

an operation mode control circuit, wherein the operation mode control circuit includes a control signal generator, a write protection circuit for latching a second output signal from the control signal generator in response to a first output signal from the control signal generator and generating a write signal responsive to the logical value of the latched second signal, a first control circuit for latching a third output signal from the control signal generator in response to the write signal and for generating a first control signal responsive to the logical value of the latched third output signal, a second control circuit for latching a fifth output signal from the control signal generator in response to a fourth output signal from the control signal generator, and for generating a second control signal responsive to the logical value of the latched fifth output signal, and an OR gate for OR gating the first control signal and the second control signal and outputting an OR gate output as an operation mode setting signal;

a signal input and output control circuit for controlling of signal inputting from and signal outputting to the outside;

a data register for latching a data signal from the operation mode control circuit in response to a data register write signal from the operation mode control circuit;

a timer for generating a clock with at least one constant period; and

a selection circuit for selecting one of the data register and the timer in response to the first control signal from the operation mode control circuit,

wherein the data register outputs a signal responsive to the data signal to the signal input and output control circuit.

17. An operation mode control circuit of a microcomputer for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator;

a write protection circuit that outputs a buffer signal that is a buffered version of a first output signal from the control signal generator when a step prior to a predetermined initialization routine phase is in progress subsequent to the commencement of an initialization program while outputting a fixed signal in the rest of the time; and

a control circuit for latching a second output signal from the control signal generator in response to the output signal from the write protection circuit,

wherein the control circuit sets an operation mode of an input and output control circuit that controls signal inputting from and signal outputting to the outside in response to the latched second output signal.

18. An operation mode control circuit as claimed in claim 17, wherein the first output signal from the control signal generator comprises a pulse signal.

19. An operation mode control circuit as claimed in claim 17, wherein the write protection circuit comprises:

a first status signal generator for generating a first status signal indicating that the initialization program is in progress;

a second status signal generator for generating a second status signal indicating that the step prior to the predetermined initialization routine phase is in progress;

a first AND gate for AND gating the first status signal and the second status signal;

a set-reset flip-flop for outputting a signal having a logical value of "1" in a reset state while outputting a signal having a logical value of "0" when the output from the first AND gate is a predetermined signal; and

a second AND gate for AND gating the first output signal from the control signal generator and the output signal from the set-reset flip-flop.

20. A microcomputer comprising:

an operation mode control circuit, wherein the operation mode control circuit includes a control signal generator, a write protection circuit that outputs a buffer signal that is a buffered version of a first output signal from the control signal generator when a step prior to a predetermined initialization routine phase is in progress subsequent to the commencement of an initialization program while outputting a fixed signal in the rest of the time, and

a control circuit for latching a second output signal from the control signal generator in response to the output signal from the write protection circuit;

an input and output control circuit for controlling signal inputting from and signal outputting to the outside; and

a data register for latching a data signal from the operation mode control circuit in response to a data register write signal from the operation mode control circuit,

wherein the data register outputs a signal responsive to the data signal to the input and output control circuit.

21. A control system comprising:

a microcomputer, wherein the microcomputer includes an input and output circuit having a plurality of operation modes, a control signal generator for generating a write signal in an operation mode setting routine of the control program, a

control circuit for setting an operation mode of the input and output circuit in response to the write signal, and a protection circuit for protecting the input and output circuit from being reset in operation mode until the protection circuit is reset by a reset signal from the outside once the control circuit has set the operation mode, a monitoring signal output port for outputting a monitoring signal to the watchdog timer, a reset signal input port for receiving a first reset signal from the watchdog timer, and

a reset circuit for generating a second reset signal to be output to a predetermined circuit of the microcomputer in response to the first reset signal; and

a watchdog timer,

wherein the output from the input and output control circuit comprises the monitoring signal supplied to the watchdog timer, and

wherein the watchdog timer outputs the first reset signal to the microcomputer.